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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/786,670	02/25/2004	Christian Eichrodt	60705-1351	3024

24504 7590 11/12/2008

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EXAMINER	
CORRIELUS, JEAN B	

ART UNIT	PAPER NUMBER
2611	

MAIL DATE	DELIVERY MODE
11/12/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/786,670	EICHRODT ET AL.	
	Examiner	Art Unit	
	Jean B. Corrielus	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10/2/08*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *15-27,29 and 31-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *19,20,26,27,29,31-34,37 and 38* is/are rejected.

7)☒ Claim(s) *15-18, 21-25, 35-36* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 10/2/08 has been entered.

Claim Objections

2. Claim 15-27, 29, 31, 35-36 and 38 are objected to because of the following informalities: Claim 15, line 10, "triggers" should be replaced by "is triggered". Claim 15, line 15, is the limitation "devices" the same as "devices", recited in line 8? If so line 15, "said/the" should be inserted before devices so as to make use of antecedent in line 8. Similar comment applies to similar limitation, recited in claim 38, line 5 with respect to the limitation recited in claim 37, line 5. Claim 19, line 2, "further" should be inserted before "comprises". Claim 20, the limitation "the clock detector further includes the current mirror and the resistor-capacitor combination is coupled to the current mirror "is redundant since such limitation is recited in claim 15.

As per claim 26, in the comment filed 10/2/08, page 7, applicant identified elements 200 of fig. 7 as the data integrity supervisor, please identify in the drawing and specification the structures corresponding to "means for monitoring" and the "means for generating" as recited in claim 26.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 19-20 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01. The omitted structural cooperative relationships are:

Claim 19, the claim fails to recite the necessary connection between the "first monostable circuit and second monostable circuit" and the previous components recited in claim 15 to form the clock detector. Claim 20 is likewise rejected because of its dependency to claim 19.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 32 and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kawasugi Seiichi Japanese Patent No. JP356143739A in view of Gunderson US patent No. 4,029,913.

As per claim 32, Kawasugi Seiichi teaches a transmission circuit fig. 2 comprising: and A/D converter and a gate circuit 17 considered as the claimed "signal integrity supervisor" configured to generate a response (output of circuit 17) to a digital

data stream having an anomalous condition see inputs to circuit 17 the gate circuit 17 (signal integrity supervisor) configured to forward the response to circuit 13 considered as the claimed " control logic" capable of resetting the transmission circuit 10 (note that, in response to the anomalous signal, a string of signals is sent to circuit 13, the string of zeros is by definition a reset signal) (see abstract). However, Kawasugi Seiichi fails to teach that the response is provided to a line driver within the transmission unit, wherein the response powers down the line driver. Gunderson teaches in system comprising a line driver being turn off in response to a shutdown signal see col. 28, lines 30-32. Given that fact, it would have been obvious to one skill in the art to include a line driver in Kawasugi and to turnoff the line driver in response to a shut down signal in order to reduce power consumption of the line driver and thereby minimize power used by the circuit.

As per claim 34, as applied to claim 32 above, Kawasugi Seiichi and Gunderson teach every feature of the claimed invention but do not explicitly teach the additional limitation the digital data stream anomalous condition is a data signal having a corresponding data value that does not vary for a predetermined maximum number of clock cycles. However, it would have been obvious to one skill in the art to configure Kawasugi Seiichi and Gunderson in such a way as set the anomalous condition as at a data signal having a corresponding data value that does not vary for a predetermined maximum number of clock cycles so as to provide proper means to identify signal abnormalities so as to provide proper compensation.

7. Claim 33 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kawasugi Seiichi Japanese Patent No. JP356143739A Gunderson US patent No. 4,029,913 and further in view of Buer US Patent No. 6,188,257.

As per claim 33, as applied to claim 32 above, Kawasugi Seiichi and Gunderson teach every feature of the claimed invention but do not explicitly teach the additional limitation of "wherein the digital data stream anomalous condition is a clock signal frequency that falls below a predetermined minimum value". Buer teaches the additional limitations of "the digital data stream anomalous condition is a clock signal frequency that falls below a predetermined minimum value". See col. 1, line 65-col. 2, line 2. Given that fact, it would have been obvious to one skill in the art to incorporate such a teaching in Kawasugi Seiichi and Gunderson so as to minimize signal processing error since the system would have been allowed to act on abnormal signal.

8. Claims 37 and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kawasugi Seiichi Japanese Patent No. JP356143739A in view of Gunderson US patent No. 4,029,913 in view of Nakatani US Patent No. 6,130,619.

As per claim 37, as applied to claim 32 above, Kawasugi Seiichi and Gunderson teach every feature of the claimed invention but does not teach the further limitation of "a clock detector configured to receive a clock signal input and generate a first output signal in response to an at least one clock signal input anomalous condition, wherein the clock detector is further configured to forward the first output signal to at least one of control logic". Nakatani teaches "a clock detector (30 and 40) configured to receive a clock signal input from clock generator 10 and generate a first output signal (see output

of circuit 40) in response to an at least one clock signal input anomalous condition (see output of circuit 30), wherein the clock detector (30 and 40) is further configured to forward the first output signal to circuit 20 (at least one of control logic) that includes a microprocessor. It would have been obvious to one skill in the art to incorporate such a teaching in Kawasugi Seiichi in order to determine abnormal conditions related to a clock signal in a communication device as to provide proper compensation.

As per claim 38, Kawasugi Seiichi teaches a transmission circuit fig. 2 comprising: and A/D converter and a gate circuit 17 considered as the claimed "signal integrity supervisor" configured to generate a response (output of circuit 17) to a digital data stream having an anomalous condition see inputs to circuit 17 the gate circuit 17 (signal integrity supervisor) configured to forward the response to circuit 13 considered as the claimed " control logic" capable of resetting the transmission circuit 10 (note that, in response to the anomalous signal, a string of signals is sent to circuit 13, the string of zeros is by definition a reset signal) (see abstract).

9. Claim 26 is rejected under 35 U.S.C. 10.3(a) as being unpatentable Hatata et al US Patent No. 4,481,629 in view of Shinozaki US patent No. 5,568,135.

As per claim 26, Hatata et al teaches a circuit comprising means 2 for monitoring a digital data stream (output of circuit 1) , wherein the means for monitoring a digital data stream comprises a consistency detecting circuit 4 (signal integrity supervisor); and Hatata includes a inherently a means for generating an output signal 4a (because in order to generate an output signal 4a, a means for generating such a signal has to be provided) in response to an anomalous condition in the digital data stream, wherein the

means for generating an output signal is responsive to a digital data stream having a number of consecutive data values of equal magnitude wherein the number of consecutive data values reaches a predetermined maximum value (3 consecutive data values) (see abstract and col. 2, lines 10-18. However, Hatata et al does not teach the further limitation of "the output signal including a fault recovery response to reset at least one component when the anomalous condition is detected". Shinozaki teaches the further limitation of the output signal including a fault recovery response to reset at least one component when the anomalous condition is detected see col. 12, lines 42-45. Given that fact, it would have been obvious to one skill in the art to incorporate such a teaching in Hatata et al so as to ensure that any corrupted signal is removed from the recovered signal so as to preserve the integrity of the original signal.

10. Claim 27 is rejected under 35 U.S.C. 10.3(a) as being unpatentable Hatata et al US Patent No. 4,481,629 in view of Shinozaki US patent No. 5,568,135 and further in view of Bartelink US patent No. 4,390,750.

As per claim 27, as applied to claim 26 above, Hatata et al and Shinozaki teach every feature of the claimed invention but do no teach the limitations of the anomalous condition would create a DC signal. As evidence by Bartelink, it is known for an anomalous condition to create a DC signal. Given that, it would have been obvious to one skill in the art to modify Hatata et al and Shinozaki in such a way to create a DC signal during an anomalous condition in order to provide proper compensation for DC offset so as to improve data detection.

11. Claim 29 is rejected under 35 U.S.C. 10.3(a) as being unpatentable Hatata et al US Patent No. 4,481,629 in view of Shinozaki US patent No. 5,568,135.and further in view of Nakatani US Patent No. 6,130,619.

As per claim 29, as applied to claim 26 above, Hatata et al Shinozaki teach every feature of the claimed invention and further teach that the signal integrity supervisor includes a data supervisor and do no teach the limitations of a clock detector included in the signal integrity supervisor. Nakatani teaches "a clock detector (30 and 40) configured to receive a clock signal input from clock generator 10 and generate a first output signal (see output of circuit 40). It would have been obvious to one skill in the art to incorporate such a teaching in Hatata and Shinozaki in order to determine abnormal conditions related to a clock signal in a communication device as to provide proper compensation.

12. Claim 31 is rejected under 35 U.S.C. 10.3(a) as being unpatentable Hatata et al US Patent No. 4,481,629 in view of Shinozaki US patent No. 5,568,135 and further in view of Buer US Patent No. 6,188,257.

As per claim 31, Hatata and Shinozaki teach every feature of the claimed invention but do not explicitly teach the means for generating an output signal is responsive to a digital data stream having a clock signal that falls below a predetermined minimum frequency. Buer teaches a method and apparatus comprising a circuit fig. 1 to generate a response "reset" to a digital data stream (note that the signal on lines 151 and 152 have to be a digital signal since such signal is provided to a digital circuit) having an anomalous condition i.e. a clock signal frequency that falls below a

predetermined minimum value. See col. 1, line 65- col. 2, line 2. Given that fact, it would have been obvious to one skill in the art to incorporate such a teaching in Hatata and Shinozaki so as to minimize signal processing error since the system would not have been allowed to act on abnormal signal.

Allowable Subject Matter

13. Claims 19-20 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action.

14. Claims 15-25, 35 and 36 would be allowable if amended to overcome the objection set forth above.

Response to Arguments

15. Applicant's arguments with respect to claims 26-27, 29, 31-34, 37 and 38 have been considered but are moot in view of the new ground(s) of rejection. Applicant argues that there is no requirement for the claims limitations to be connected. However, MPEP 2172.01, partially states that:

In addition, a claim which fails to interrelate essential elements of the invention as defined by applicant(s) in the specification may be rejected under 35 U.S.C. 112, second paragraph, for failure to point out and distinctly claim the invention. See *In re Venezia*,

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jean B. Corrielus whose telephone number is 571-272-3020. The examiner can normally be reached on Monday-Thursday from 9:30-3:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh Fan can be reached on 571-272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Jean B Corrielus/
Primary Examiner
Art Unit 2611